What is claimed is:

1. A method of producing a bipolar transistor, comprising:

providing a semiconductor substrate having a substrate surface;

forming a base-terminal layer on the substrate surface for providing a base terminal;

forming an emitter window, comprising a wall area, in the base-terminal layer;

forming a first spacing layer on the wall area of the emitter window;

etching a recess in the semiconductor substrate within a window specified by the first spacing layer;

forming a base layer in the recess of the emitter window;

forming a second spacing layer on the first spacing layer and on the base layer;

structuring the second spacing layer for the purpose of specifying a planar terminal pad on the base layer;

forming an emitter layer on the planar terminal pad.

2. The method as claimed in claim 1, wherein in the step of forming the first spacing layer, the wall area of the emitter window is fully covered, so that after the step of forming the base layer, the base-terminal layer does not touch the base layer.

3. The method as claimed in claim 1, wherein the first spacing layer is formed by means of deposition.

4. The method as claimed in claim 1, wherein the step of etching the recess includes a step of anisotropic dry-etching into the substrate.

5. The method as claimed in claim 4, wherein the step of etching the recess includes a further step of isotropic wet-etching performed after the step of the anisotropic dry-etching.

6. The method as claimed in claim 1, wherein the base layer is formed by selective epitaxial deposition.

7. The method as claimed in claim 1, wherein the step of forming the base layer includes a further step of forming an isolation layer on the base layer, the emitter window being formed in the base-terminal layer and in the isolation layer.

8. The method as claimed in claim 1, wherein the emitter layer is formed by depositing a poly- or monosilicon.

9. The method as claimed in claim 1, wherein the base-terminal layer is formed by depositing a doped polysilicon layer.

10. The method as claimed in claim 9, wherein a conductive connection between the base layer and the base-terminal layer is produced by diffusing a dopant out of the base-terminal layer.

11. A bipolar transistor, comprising:

a semiconductor substrate;

a base-terminal layer arranged on the semiconductor substrate;

a further recess extending through the base-terminal layer into the semiconductor substrate;

a first spacing layer arranged on walls of the further recess;

a base layer arranged in the further recess;

a second spacing layer which is arranged on the first spacing layer and the base layer and specifies a planar terminal pad on the base layer;

an emitter layer arranged on the planar terminal pad.

12. Bipolar transistor as claimed in claim 11, wherein the first spacing layer is formed to separate the base layer from the base-terminal layer in a wall area of the further recess.

13. The bipolar transistor as claimed in claim 11, wherein the base-terminal layer is a doped polysilicon.

14. The bipolar transistor as claimed in claim 11, wherein the further recess comprises an area which is arranged underneath the base-terminal layer.

15. The bipolar transistor as claimed in claim 13, wherein the base layer and the base-terminal layer are conductively connected essentially by means of a dopant diffused out of the base-terminal layer.

16. The bipolar transistor as claimed in claim 11, wherein the emitter layer comprises doped poly- or monosilicon.

17. The bipolar transistor as claimed in claim 11, wherein an isolation layer is arranged on the base-terminal layer, the emitter window extending through the isolation layer and through the base-terminal layer.

18. The bipolar transistor as claimed in claim 11, which comprises a shallow trench isolation.